C-MOS Gate-Array TS046

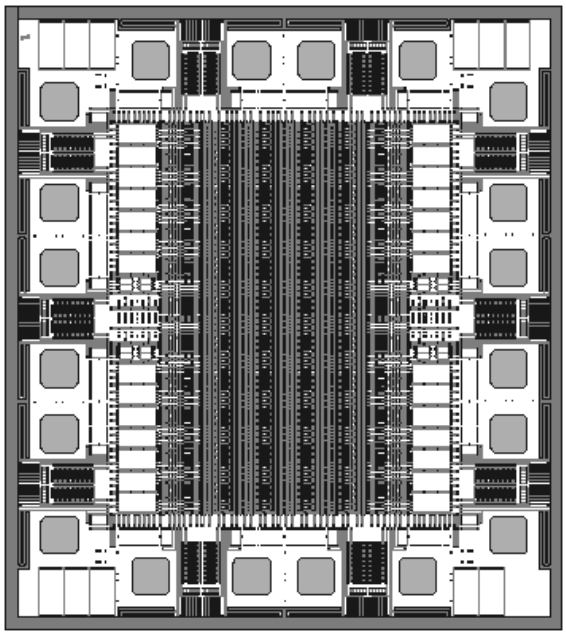
DESCRIPTION

The TS046 is a semicustom masterchip built in a single metal C-MOS technology. The main application of this component array is to realize mixed-signal ASICs (Application Specific Integrated Circuits) of moderate complexity in a rather short development time and with low development costs. The chip contains a lot of different active and passive components which can be interconnected by a single customized metal mask. Half of the TS046 is a gate-array structure which is mainly used for digital circuits. The other half is the analog section containing 4 identical tiles with transistors of different sizes, diodes, resistors and capacitors. This part can be used to realize numerous analog functions. The available components and the low threshold voltage of the employed C-MOS process make the TS046 specially suited to build low current and low voltage circuits.

FEATURES

- Digital part: 464 transistor pairs (N-MOS and P-MOS)
- Analog part: Separate N-MOS and P-MOS transistors, diodes, low and high value resistors, floating capacitors
- 20 input/output cells
- Programmable by a single metal mask Very flexible wiring possibilities
- Processed with the proven SACMOS technology of PHILIPS SEMICONDUCTORS
- Supply voltage range: 0.9V to 6.5V
- High speed operation: min. 100MHz toggle frequency at V_{DD} = 4.5V
- Small chip size: 1.45mm x 1.66mm Encapsulation in SO8 package possible

LAYOUT



CROSSMOS LTD
Rue de la Gare 15b
CH-2074 Marin
Switzerland

Phone: +41 32 753 6272
Fax: +41 32 753 6109
Mail: info@crossmos.ch
Web: www.crossmos.ch

October 2004

C-MOS Gate-Array TS046

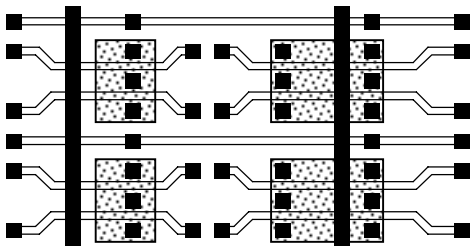
SHORT PROCESS DESCRIPTION

- N-well silicon-gate C-MOS process
- Low ohmic substrate with epitaxial layer guaranties a latch-up free circuit behaviour
- 2µm feature size
- Self aligned contacts (SAC) results in a 4µm unrestricted pitch for metal interconnections
- Low threshold voltage: 0.60V ± 0.15V for N-MOS and P-MOS transistors
- Operating voltage range: 0.9V to 6.5V. Maximum rating: 7.0V
- Sheet resistance of polysilicon: 30Ω/square
- Sheet resistance of metal: 25mΩ/square

DIGITAL PART

- 464 transistor pairs standard sized (N: 10/2 P: 16/2)
- 20 input/output cells
- The basic transistor pairs can be connected with the metal mask into NOR and NAND gates with any number of inputs, into transmission gates, combined logic functions, latches, flip-flops, etc.
- Organized in 4 rows of 116 transistor pairs each
- Routing channels with 9 interconnect lines between the logic rows

Layout of the basic transistor pair structure



CROSSMOS LTD
Rue de la Gare 15b
CH-2074 Marin
Switzerland

Phone: +41 32 753 6272
Fax: +41 32 753 6109
Mail: info@crossmos.ch
Web: www.crossmos.ch

ANALOG PART

MOS TRANSISTORS

Size	Width (µm)	Length (µm)	Number (N and P each)
A	6	5	80 x 3
H	3	30	8 x 2
F (N)	4 x 18	5	8 (N only)
F (P)	4 x 36	5	8 (P only)

There are three different transistor geometries in the analog part.
The transistors of size A are mainly used for amplifiers and comparators. The 5µm gate length results in a lower offset voltage and higher gain fo the amplifier than the standard 2µm gate lenth. The long and narrow transistors of size H are used to build current mirrors with a large multiplication ratio, low value current sources or high impedance resistors. The finger size F transistors are used for input differential pairs of operational amplifiers in order to minimize the offset voltage.
The N-well of the P-MOS is divided into several isolated regions, allowing an optimum circuit design in case of different supply voltages (e.g. for voltage doublers, separate LCD supply, etc.).

DIODES

40 single emitter bipolar PNP substrate transistors are provided. They are mainly foreseen for temperature compensated bandgap voltage references.
Diode voltage (emitter-base voltage) @ T_{amb} = 25°C:
$V_D = 26mV \times \ln(I_D / I_S) + R_{eq} \times I_D$ with I_S = 0.1fA and R_{eq} = 150Ω

RESISTORS

Value (kΩ)	Number	Tolerance (%)	TC (%/°C)
1	192	-25 +25	0.1
30	84	-30 +40	0.5
300	14	-30 +40	0.5

CAPACITORS

	Size 1	Size 2
Maximum floating capacitance	3pF	5pF
Substrate capacitance	0.25pF	0.4pF
Number of areas	28	11

The floating capacitors are built between the polysilicon and the metal, in areas where the polysilicon is covered only by a thin oxyde layer which results in a high specific capacitance of 850pF/mm^2. The value of the capacitors is programmed by the size of the metal plate.

CROSSMOS LTD
Rue de la Gare 15b
CH-2074 Marin
Switzerland

Phone: +41 32 753 6272
Fax: +41 32 753 6109
Mail: info@crossmos.ch
Web: www.crossmos.ch

PERIPHERY

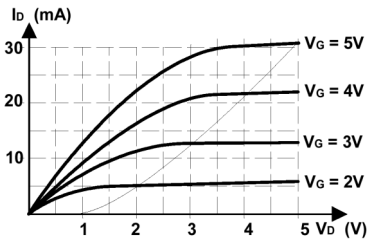
The periphery consists of 20 identical cells containing one pad, three buffer transistors (2 N-MOS and 1 P-MOS) and two 15kΩ pullup/pulldown resistors. Each cell is programmable as supply, as input, as push-pull output, as open-drain output or as bidirectional I/O pin. The output transistors can also be connected as transmission gates. The transistors of adjacent cells can be connected together to increase the output drive capability.

The electrostatic discharge (ESD) structure which protects the pin against overvoltage is realized by one of the N-MOS having his source always connected to V_{SS}. This structure sustain ESD test pulses of more than 2kV (Generator impedance: 100pF, 1.5kΩ)

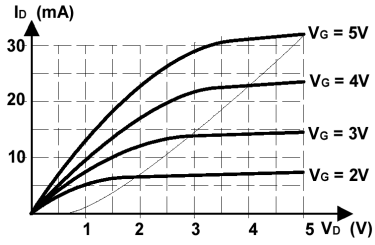
Size of the output transistors:	N-Buffer	192µm / 2.0µm
	P-Buffer	512µm / 2.0µm
	N-Protection	264µm / 2.2µm

Typical characteristics of the output transistors

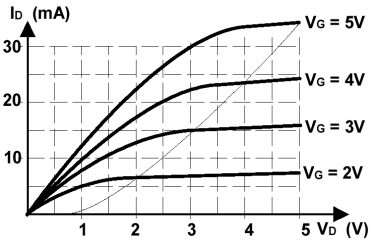
N-Buffer



P-Buffer



N-Protection



CROSSMOS LTD
Rue de la Gare 15b
CH-2074 Marin
Switzerland

Phone: +41 32 753 6272
Fax: +41 32 753 6109
Mail: info@crossmos.ch
Web: www.crossmos.ch