C-MOS Gate-Array SM003

DESCRIPTION

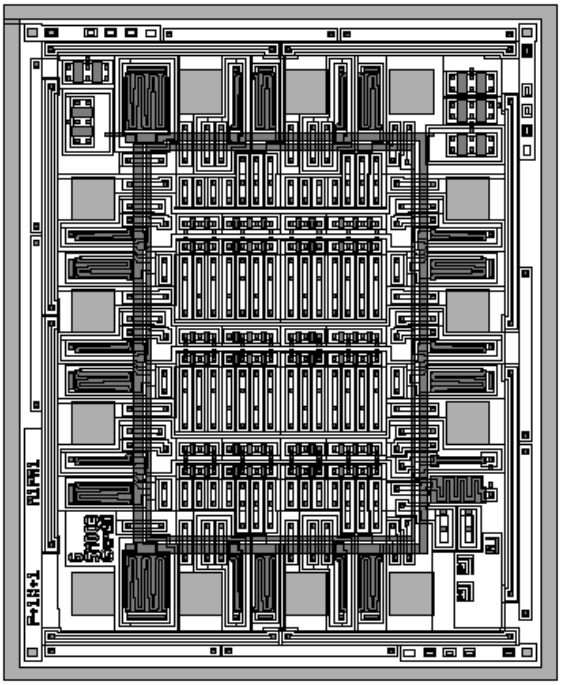
The SM003 is a semicustom masterchip built in a single metal C-MOS technology. The main application of this component array is to realize mixed-signal ASICs (Application Specific Integrated Circuits) of small complexity in a very short development time and with very low development costs. The chip contains different active and passive components which can be interconnected by a single customized metal mask. The larger part of the SM003 has a gate-array structure which can be used for digital circuits as well as for numerous analog functions. Some high value resistors allow to control low current sources. The available components, the low threshold voltage and the high breakdown voltage of the employed C-MOS process make the SM003 specially suited to build high voltage, high noise immunity and low current circuits.

The SM003 is the smallest Gate-array in the World.

FEATURES

- Active components: 30 transistor pairs for use in analog or digital functions (N-MOS and P-MOS)
- Passive components: diodes, low and high value resistors, zener diodes
- 13 input/output cells
- Programmable by a single metal mask Very flexible wiring possibilities
- Processed with the proven Metal-gate technology of SEMEFAB (4'000 serie)
- Supply voltage range: 0.9V to 18V
- High noise immunity
  Ideal for industrial environment
- Medium speed operation: min. 5MHz toggle frequency at V_{DD} = 4.5V
- Small chip size: 50mils x 61mils
  (1.3mm x 1.6mm)
- Encapsulation in SO8 package possible

LAYOUT



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October 2004

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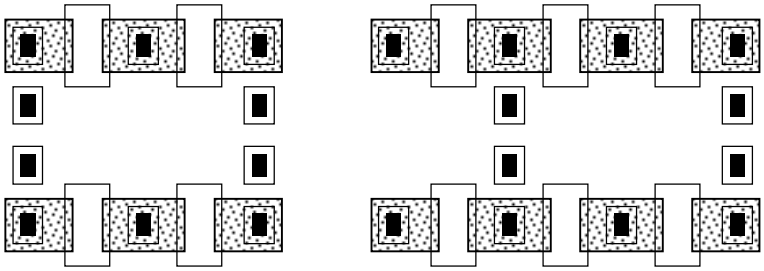
SHORT PROCESS DESCRIPTION

- P-well metal-gate C-MOS process
- Low ohmic diffusions on substrate and well guarantie a latch-up free circuit behaviour
- 6µm feature size
- High breakdown voltages and channel stoppers around all transistors allow a high voltage operation
- Low threshold voltage: 0.80V ± 0.2V for N-MOS and P-MOS transistors
- Operating voltage range: 0.9V to 18V. Maximum rating: 24V
- Sheet resistance of diffusions: N_+ = 12Ω/square, P_+ = 110Ω/square
- Sheet resistance of metal: 35mΩ/square

DIGITAL PART

- 30 transistor pairs standard sized (N: 14/6 P: 14/6). It's the smallest in the World !
- 4 transistor pairs with greater dimensions (N: 40/20 P: 40/20) specially suited for differential stage of comparators or operational amplifiers
- 13 input/output cells
- The basic transistor pairs can be connected with the metal mask into NOR and NAND gates with any number of inputs, into transmission gates, combined logic functions, latches, flip-flops, etc.
- Organized in 3 columns of 10 transistor pairs each
- Routing channels with 9 interconnect lines between the logic rows

Layout of the basic transistor pair structure



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ANALOG PART

MOS TRANSISTORS

All digital transistors of the array can be used for analog circuitry. The 8µm gate length results in a low offset voltage and high gain fo the amplifier. They can be used for amplifiers, comparators, oscillators as well as for digital gates. N-MOS and P-MOS have separated gate connections and provide therefore a maximum of flexibility for the routing.
The P-well of the N-MOS is divided into several isolated regions, allowing an optimum circuit design in case of different supply voltages (e.g. for voltage doublers, separate LCD supply, etc.).

DIODES

Several single and multi-emitter bipolar NPN substrate transistors are provided by unused diffusions in unused P-wells. They can be used for temperature compensated bandgap voltage references. Their small emitter area provides a higher current density for low power applications.

RESISTORS

Value (Ω)	Number	Tolerance (%)	TC (%/°C)
260	42	-10 +10	0.01
6.5k	8	-10 +10	0.01
250k	8	-30 +30	0.20

CAPACITORS

	Underpass
Substrate capacitance	0.45pF @0V, 0.32pF @5V
Number of areas	42

The substrate capacitors are junctions between the P-diffusions (underpasses) and the N-substrate. Their value depends on the applied voltage like a varicap. They allow nevertheless to build oscillators, monoflops or other types of delays.

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PERIPHERY

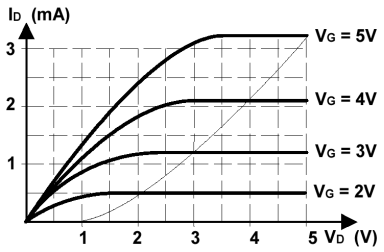
The periphery consists of cells containing one pad and either buffer transistors (1 N-MOS and 1 P-MOS) or a driver transistor (N-MOS). Each cell is programmable as supply, as input, as push-pull output, as open-drain output or as bidirectional I/O pin. The output transistors can also be connected as transmission gates. The transistors of adjacent cells can be connected together to increase the output drive capability.
An electrostatic discharge (ESD) structure which protects the pin against overvoltage is also part of each periphery cell. This structure sustain ESD test pulses of more than 2kV (Generator impedance: 200pF, 1kΩ)

There are 9 buffer cells and 2 driver cells

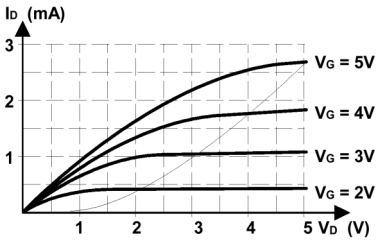
Size of the output transistors:	N-Buffer	126µm / 8µm
	P-Buffer	380µm / 8µm
	N-Driver	750µm / 8µm

Typical characteristics of the output transistors

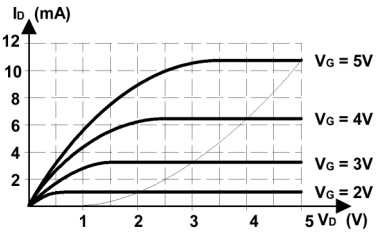
N-Buffer

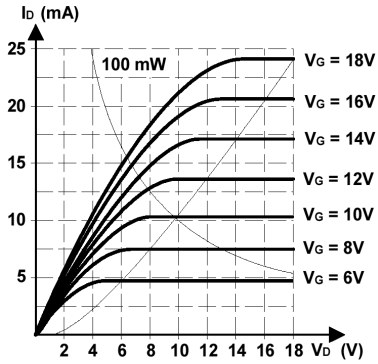


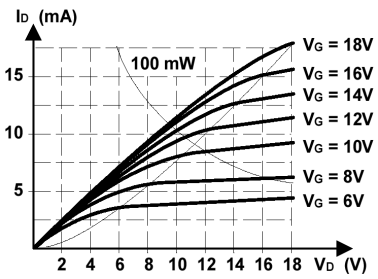
P-Buffer

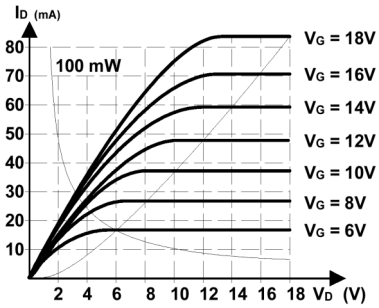


N-Driver









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